

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				M-15170 US		10/624,965	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)			
(Use several sheets if necessary)				Kevin E. Sallesse			
				Filing Date		Group	
				07/21/2003		2183	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AL						
	AM						
	AN						
	AO						
	AP						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
DC	AQ	Streamline Design Efforts With The New SPI4-2 Interface, by John Deatherage, Intel Developer UPDATE Magazine, September 2002, PP. 1-6.					
DC	AR	3.3V Programmable Skew PLL Clock Driver Turboclock, IDT5V991A, Commercial and Industrial Temperature Ranges, September 2001, PP. 1-10					
DC	AS	One-PLL General Purpose Flash-Programmable Clock Generator, CY22050, Cypress Semiconductor Corporation, San Jose, CA, Revised December 14, 2002, PP. 1-8					
Examiner		Date Considered					
DC		12/28/04					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

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DC	AQ	ICS541, PLL Clock Divider, Revision 021303, Integrated Circuit Systems, Inc., PP. 1-5, No date					
SC	AR	User Programmable Laser Engine Pixel Clock Generator, ICS1574B, 08/31/2000, PP. 1-12					
DC	AS	EEPROM Programmable 3-PLL Clock Generator IC, FS6370-01, AMI Semiconductor, PP. 1-39, No date					
Examiner		Date Considered					
D. D. Chen		12/28/04					
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